COMPLETE LISTING OF THE CLAIMS

The following lists all of the claims that are or were in the above-identified patent application. The status identifiers respectively provided in parentheses following the claim numbers indicate the current statuses of the claims.

1. (Currently Amended) A probing system for testing a device comprising:

a probe comprising a semiconductor die and probe tips rigidly attached to the semiconductor die, wherein the probe tips comprise bumps that are arranged in a pattern that matches a pattern of terminals on the device and that directly contact the terminals during testing of the device, the probe tips being affixed to the semiconductor die so that the pattern of the probe tips expands/contracts with thermal expansion/contraction of the semiconductor die;

a substrate on which the semiconductor die is mounted;

a probe card including a receptacle sized to hold the substrate, wherein the substrate is detachably mounted in the receptacle; and

a tester electrically connected to the probe tips.

2. (Original) The system of claim 1, wherein the device comprises a semiconductor material that is substantially the same as material in the semiconductor die.

3. (Canceled)

4. (Canceled)

5. (Currently Amended) The system of ~~claim 4~~ claim 1, wherein the substrate is substantially identical to a substrate used in a flip-chip package for the device.

6. (Canceled)

7. (Original) The system of claim 1, wherein the semiconductor die comprises:

terminals on a bottom surface of the semiconductor die; and

conductive vias that pass through the semiconductor die and provide electrical connections between the probe tips on a top surface of the die and the terminals on the bottom

PATENT LAW OFFICES OF
DAVID MILLERS
6560 ASHFIELD COURT
SAN JOSE, CA 95120
PH: (408) 927-6700
FX: (408) 927-6701

surface.

8. (Currently Amended) The system of claim 7, ~~wherein the probe further comprises a substrate on which the semiconductor die is mounted,~~ wherein the terminals of the semiconductor die directly contact the substrate.

9. (Currently Amended) The system of claim 8, ~~further comprising a probe card,~~ wherein terminals on the substrate directly contact the probe card.

10. (Original) The system of claim 1, further comprising a positioning system adapted to position the probe relative to the device so that the probe tips contact the terminals on the device.

11. (Canceled)

12. (Canceled)

13. (Currently Amended) A method for forming a probe for electrical testing of a semiconductor device, comprising:

forming probe tips on a first surface of a semiconductor die in a pattern matching a pattern of ~~terminals~~ contacts on the semiconductor device, wherein forming the probe tips comprises:

forming contact pads directly on the semiconductor die; and

forming conductive bumps on a surface of the contact pads, wherein tops of the conductive bumps provide surfaces that during testing directly contact the ~~terminals~~ contacts of the semiconductor device;

forming terminals on a second surface of the semiconductor die in a pattern matching the pattern of the contacts on the semiconductor device; and

forming conductive vias through the semiconductor die, wherein the conductive vias electrically connect the probe tips respectively to the terminals. ~~fabricating an interconnect structure for electrical connection of the probe tips to test equipment~~.

14. (Canceled)

15. (Canceled)

PATENT LAW OFFICES OF
DAVID MILLERS
6560 ASHFIELD COURT
SAN JOSE, CA 95120
PH: (408) 927-6700
FX: (408) 927-6701

16. (Canceled)

17. (Canceled)

18. (Currently Amended) The method of ~~claim 17~~ claim 13, wherein forming the conductive vias comprises:

forming holes in the semiconductor die; and

filling the holes with a conductive material.

19. (Previously Presented) The method of claim 18, wherein forming the holes comprises laser drilling.

20. (Previously Presented) The method of claim 18, wherein forming the holes comprises etching.

21. (Currently Amended) The method of ~~claim 17~~ claim 13, wherein forming the conductive vias comprises forming doped regions that extend through the semiconductor die.

22. (Canceled)

23. (Currently Amended) The method of ~~claim 22~~ claim 13, further comprising attaching the terminals to an interconnect substrate.

24. (Previously Presented) The method of claim 23, wherein attaching the terminals comprises performing a solder reflow process.

25. (Previously Presented) The method of claim 13, wherein forming probe tips further comprises planarizing the bumps.

26. (Previously Presented) The method of claim 25, wherein planarizing comprises chemical mechanical polishing of the bumps.

27. (Previously Presented) The method of claim 13, forming contact pads on the semiconductor die comprises a manufacturing process that is substantially identical to a

PATENT LAW OFFICES OF
DAVID MILLERS
6560 ASHFIELD COURT
SAN JOSE, CA 95120
PH: (408) 927-6700
FX: (408) 927-6701

process used in fabricating contact pads on the semiconductor device to be tested.

28. (Previously Presented) The method of claim 27, wherein the manufacturing process uses a mask that is substantially identical to a mask used in fabricating the contact pads on the semiconductor device to be tested.

29. (Previously Presented) The system of claim 1, further comprising contact pads that are directly on the semiconductor die, wherein the bumps respectively reside on the contact pads.

30. (Previously Presented) The system of claim 29, wherein the contact pads have a pattern identical to corresponding contact pads on the device tested.

31. (Previously Presented) The system of claim 1, wherein surfaces of the bumps that contact the device are planar and in the same plane.

32. (Previously Presented) The system of claim 1, wherein the semiconductor die is substantially identical to the device.

33. (Previously Presented) The system of claim 1, wherein the bumps are of a type suitable for use in a flip-chip package.

34. (New) The system of claim 5, wherein the semiconductor die comprises:

terminals on a bottom surface of the semiconductor die arranged in a pattern that matches the pattern of the terminals on the device; and

conductive vias that pass through the semiconductor die and provide electrical connections between the probe tips on a top surface of the semiconductor die and the terminals on the bottom surface.

PATENT LAW OFFICES OF
DAVID MILLERS
6560 ASHFIELD COURT
SAN JOSE, CA 95120
PH: (408) 927-6700
FX: (408) 927-6701

35. (New) The system of claim 1, wherein solder attaches the semiconductor die to the substrate.